[[1]](#footnote-1)

**Abstract:**

**VLSI Report – Batch 1**

**Energy Dissipation Analysis in Sequential Circuits using QCA and QCA Pro**

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In recent days, there are many alternate technologies at the nanoscale, which try to replace the most common conventional CMOS technology. The reason, behind searching for a replacement is that it takes a bit more area, and the energy dissipation is high. Out of all these new technologies the better and more efficient one is QCA[Quantum-dot Cellular Automata]. This QCA technology totally depends on a very new physical phenomenon called Columbic interactions. Columbic interactions are nothing but, electrical charges - electrostatic interactions. By using this concept, there are many advantages of designing a circuit using QCA instead of conventional CMOS technology such as Energy Dissipation[In QCA energy dissipation is less than that of CMOS technology], Area occupied by the circuit[QCA occupies less area than that of CMOS], latency or the delay between input and output[QCA have delay compared to CMOS].

Basically, in this paper, the part we are going to concentrate on is sequential circuits such as SR Latch and D Latch. We will show the energy dissipation analysis of SR Latch and D Latch. After performing all the simulations we came to an analysis that SR Latch occupies around 0.1μ of area, with 72 QCA cells and the delay or latency between input and output is 2 clock cycles. Same, after performing the simulations for D Latch, we observe that it occupies around 0.04μ of area, with 29 QCA cells, and the delay or latency between input and output is 1 clock cycle. For D Latch, we got average energy dissipated values as 0.02030meV for 0Kelvin Temperature, 0.04030meV for 5Kelvin, 0.04120meV for

10Kelvin and finally 0.04572meV for 15Kelvin. For SR Latch, we got average energy dissipation values as 2.07meV for 0K(kelvin), 2.41meV for 5K(kelvin), 2.82meV for 10K(kelvin) and 2.97meV for 15K(kelvin).

**Introduction:**

As we know, since 1965, CMOS[Complementary Metal Oxide Semiconductor] Technology follows, Moore’s law. Moore’s law states that for every 2-3 years, number of transistors on the device gets doubled. It also states that the feature size and energy dissipation shrinks at a rate of 30% for every 2-3 years. But Mr. Moore already mentioned that this trend doesn’t follow forever. Because there are many limitations, because of shrinking the feature size of CMOS to a submicron. There are also challenges such as unwanted leakage current and short channel effects, which are creating an obstruction for further decrement of feature size in CMOS circuits.

So, as this many limitations are occurred, we cannot make up to nanoscale level by using conventional CMOS technology. Hence, we need a device in which there are no limitations of this type in nano scale level. In 1993, Dr. Craig S.Lent came up with a technology called QCA[Quantum-dot Cellular Automata] at university called Notre Dame.

The main reason of considering this as an alternative approach upon CMOS technology in terms of nanotechnology is, the QCA cell size is way more less than that of a transistor. Mainly, QCA works on the technology called quantum mechanical tunnelling. Now-a-days, if we observe any electronic device or product, all they want is less in size and area, mainly energy dissipation should be low. The reason behind concentrating only on sequential circuits is because they are most used circuits in daily devices. QCA is a technology which is not at all same as CMOS technology, it uses a physical phenomenon called columbic interactions between the electrons of a cell.

**What is QCA? [Quantum dot Cellular Automata]:**

QCA is the new technology in which we will use binary states. These states are not considered as +V or –V volts, else they are considered according to the place where individual electron is located in a cell. To represent these stages we use +1 and -1 in QCA software. A cell in QCA contains 4 electrons in it. They are represented as quantum dots.

**QCA Cell:**

In this QCA the main thing which handles everything is a QCA cell. It is the fundamental unit of QCA software. It works with the logic of columbic interactions. Every cell is represented as +1 or -1 charge. ‘+1’ represents the binary logic is ‘1’ and ‘-1’ represents the binary logic is ‘0’. A cell contains 4 quantum dots placed at corners of the cell. These dots are made using some semiconductor nanoscale material, that shows up all the quantum effects. In these 4 dots, we have 2 dots which are electrons and they are always diagonally and opposite to each other because if they aren’t opposite, repulsions will be more. I mean if the electrons are adjacent to each other, the repulsions will be more when compared to electrons when they are opposite to each other. To connect this quantum dots, tunnel junctions are made.

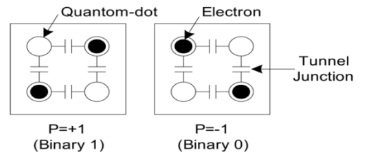


Figure 1: QCA Cell and its polarization states

The main thing which we need to understand is tunneling take place between dots when we apply some voltage. If we don’t apply any voltage the electron don’t come out of its dot. However, the electrons doesn’t leave and go out of the its cell, hence this is the main advantage of QCA and because of this energy dissipation will be less.

**QCA Wire:**

A QCA wire is placement of all few QCA cells along a same line side by side or adjacent to each other. Electrons occupy their respective positions in a cell depending upon the electrostatic forces which are acting upon them. If an electron is placed on the right top corner of a cell, the next cell electron will not be placed on left corner top because there will be repulsions, hence they will be in left bottom dot. Hence, in a wire the logic whatever we apply at the start of the wire, it travels through the wire and output is also expected the same.

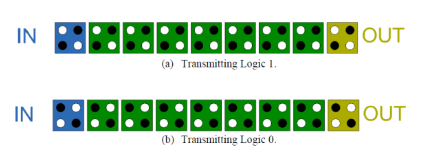


Figure 2: Transmitting logic using QCA wire

In QCA Software, we can assign the cell in two ways, in the sense we can rotate the cell. But, if we rotate the cells also, the electrons always take its position in opposite dots also, because of repulsions. So, for suppose if we rotate the cells for 450 then, the output is inverted version of input. This is the main advantage of QCA, we don’t need any separate invertor, we can directly design by using QCA cells.

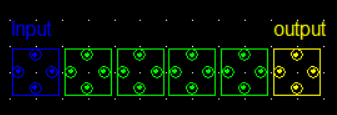


Figure 3: QCA wire with 450 rotation of cell

**QCA Wire Crossing:**

In QCA wire crossing can be done in two ways. One is Coplanar and multi-layer. In CMOS technology, wire crossings are done by making one of the wire as a bridge from the plane.

**Coplanar Wire Crossing:**

In this, wire crossing is done in the single layer. What we do is, the horizontal wire lines will have the regular cells, but the vertical wire lines will have 900 rotated cells. Such that, there will be no interaction between horizontal and vertical wire line. But there is a disadvantage of this coplanar wire crossing, that is misalignment of QCA cells, which can lead to wrong outputs.

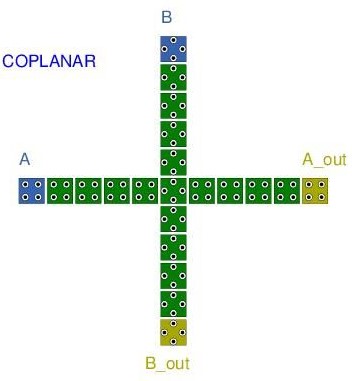


Figure 4: Coplanar Wire Crossing

**Multilayer Wire Crossing:**

In this type of wire crossing what we try to do is, we try to make a bridge type structure using multiple layers in QCA software. In first layer we will place the horizontal wire and the in the middle layer we will just keep one cell on each of the edge of horizontal wire, such that it acts like a pillar of a bridge. In last layer, we will connect the pillars using QCA cells, it acts like a bridge.

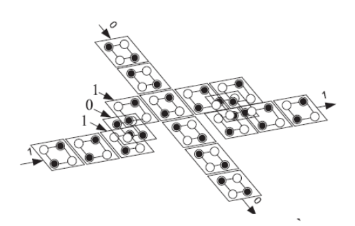


Figure 5: Multilayer Wire Crossing

**Logic Gates in QCA:**

As we know, we have logic gates such as Majority gate, AND gate, OR gate etc.

**Majority Gate:**

It gives the output majority bit from the inputs. For example, if the input values of X,Y,Z is ‘1’,’0’,’1’. The output is’1’, because majority number of bits are ‘1’. Majority gate follows.

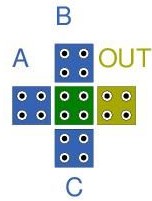


Figure 6:Majority Gate

**And Gate:**

In and gate the output is obtained by using and operation. For example, If any one of the inputs contains ’0’ then the output is ‘0’.

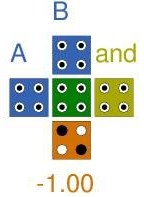


Figure 7: AND Gate

|  |  |  |
| --- | --- | --- |
| **Input P** | **Input Q** | **Output O** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Table 1: AND Gate Truth Table

**OR Gate:**

In Or gate, the output is obtained by using or operation. For example, if any one of the input is ‘1’ then the output is ‘1’.

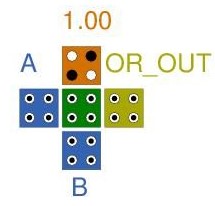


Figure 8: OR Gate

|  |  |  |
| --- | --- | --- |
| **Input L** | **Input M** | **Output R** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Table 2: OR Gate Truth Table

Now, we have completed about Simple Logic Gates in QCA. Lets now discuss, how QCA works from inside, in the backend of the QCA. It has a clock theory and everything is based on that only.

**QCA Clock Theory:**

Basically, In QCA software there is a mechanism called clocking mechanism. It regulates how information is synchronized in a particular QCA circuit. In a QCA clock there are 4 clock phases namely: Switch, hold, release and relax.

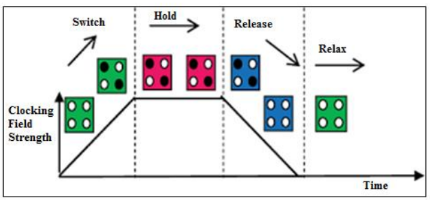


Figure 9:QCA clock phases

So, these four QCA clock phases are utilized whenever the clock signal is applied to a QCA cell. Initially in the switch case, the strength of the clock field increases and cell also starts polarizing. Next, comes Hold phase, in this the strength of field goes to maximum and cell also gets fully polarized. The QCA cell will reach its logical state of "0" or "1" during this phase. Then comes release phase, now strength of field gets gradually decreased and also QCA cell gets depolarized. In very last phase, that is relax phase, strength of the field will be minimum and QCA cell also gets completely depolarized.

**SR Latch and D Latch:**

Firstly what is a Latch? It is nothing but a basic memory unit which has an ability to store only one bit at a time. To implement these two latches in QCA, the parameters which we considered are as:

|  |  |
| --- | --- |
| **Parameter** | **Value** |
| Width | 18 |
| Height | 18 |
| Diameter of Quantum Dot | 5 |
| Time for relaxation(sec) | 1.0e-15 |
| Total time for simulation(sec) | 7.0e-11 |
| Amplitude factor of clock | 2.0 |

Table 3: QCA Cell Coherence engine simulation parameters

Now, we designed a QCA circuit of SR Latch and D Latch as shown in figure 10 and figure 11. SR latch input and output is as follows:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S** | **R** | **Q** | **Q’** | **State** |
| 1 | 0 | 1 | 0 | Set State |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | Reset State |
| 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | undefined |

**Table 4: SR latch truth table**

If we talk about D Latch, we have only one input that is D input and only one output. The truth table for truth is as follows:

|  |  |
| --- | --- |
| **Input D** | **Output** |
| 0 | 0 |
| 1 | 1 |

**Table 5: D latch truth table**

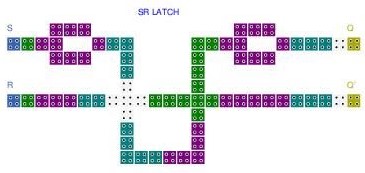
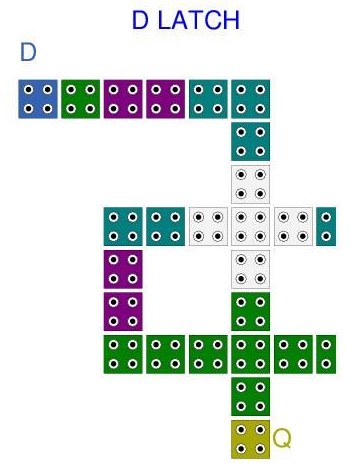


Figure 10: SR Latch QCA circuit

Figure 11: D Latch QCA circuit

**Simulation Results of SR Latch and D Latch:**

For simulation, we used QCADesigner tool, which will give output in the form of a graph, and there might be a delay or l atency between input and output.

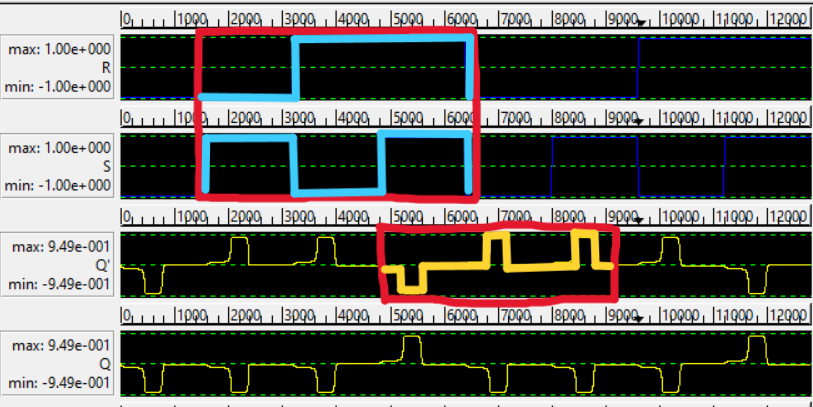


Figure 12: SR Latch Simuation output

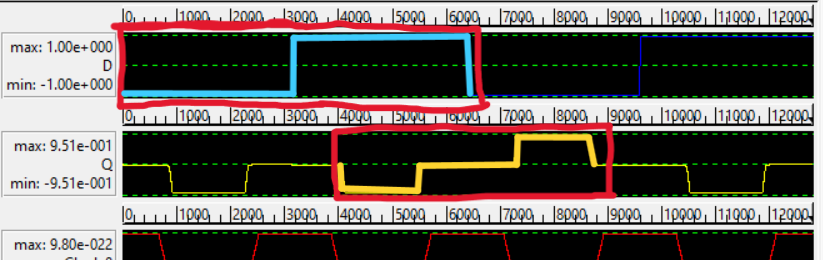


Figure 13: D Latch Simulation Output

**Energy Dissipation Analysis:**

To Analize, Energy Dissipation values at different temperatures such as 0K(kelvin), 5K(kelvin), 10K(Kelvin), 15K(Kelvin), we used software’s such as QCAPro and QCADesignerE. Whenever a clock is applied to a input of a QCA circuit,[clock has either 0 or 1] it will consider 0 or 1. Then it starts traversing from input to output part, so because of some columbic interactions between the electrons in a QCA cell, some energy dissipation may happen. This is one of the main parameter to be analized in QCA.Table 6, represents average energy dissipation of SR Latch using QCADesignerE at different temperatures.

At 0K- 2.07meV , 5K- 2.41meV, 10K- 2.82meV, 15K-2.97meV.

|  |  |
| --- | --- |
| **Temperature (Kelvin)** | **Average Energy Dissipation**  **of D Latch (meV)** |
| 0k | 2.07 |
| 5k | 2.41 |
| 10k | 2.82 |
| 15k | 2.97 |

**Table 6: Average Energy Dissipation of SR Latch QCA circuit**

Table 7, represents average energy dissipation of D latch at different temperatures. At 0K- 0.02030meV , 5K- 0.04030meV, 10K- 0.04120meV, 15K- 0.04572meV.

|  |  |
| --- | --- |
| **Temperature (Kelvin)** | **Average Energy Dissipation**  **of D Latch (meV)** |
| 0k | 0.02030 |
| 5k | 0.04030 |
| 10k | 0.04120 |
| 15k | 0.04572 |

Table 7: Average Energy Dissipation in D Latch QCA circuit

By observing both the tables we can say that, Average energy dissipation is gradually increasing as temperature is increasing. Figure 14, represent Plot between temperature and average energy dissipation of SR Latch and Figure 15, represents plot between temperature and average energy dissipation of D Latch QCA circuit.

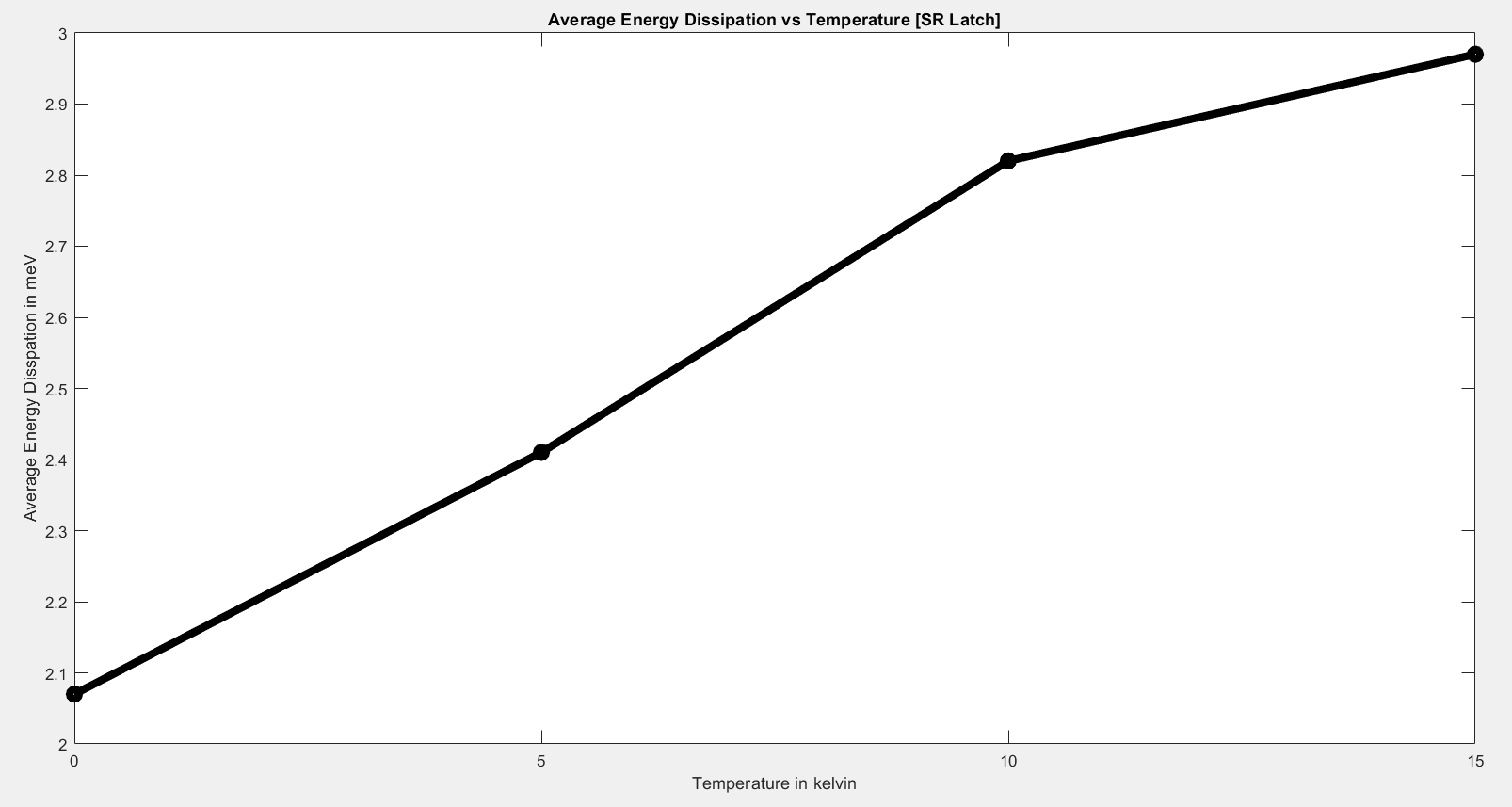


Figure 14: Plot between Average Energy Dissipation and Temperature of SR Latch

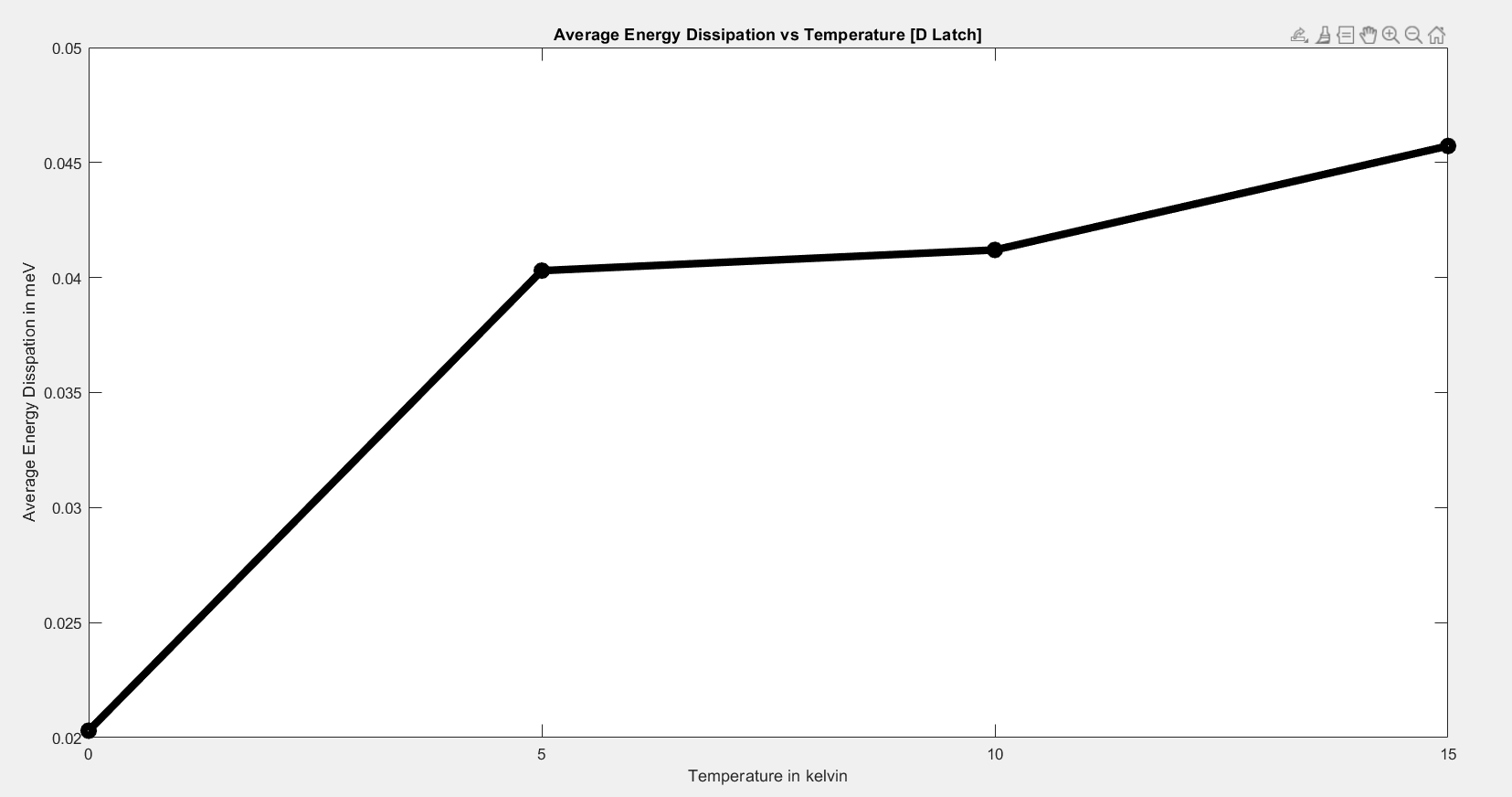


Figure 15: Plot between Average Energy Dissipation and Temperature of D Latch

By using QCA pro Software, we also depicted power dissipation picture. The cell with thick orange or brown represents more columbic interactions between electrons in that circuit, so more heat dissipated, and the cell with light yellow or orange represents less power dissipated.

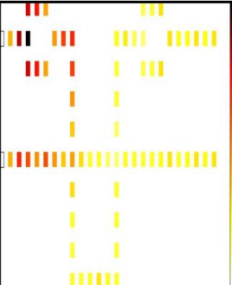


Figure 16: Thermal Energy Dissipaion Analysis of SR Latch using QCA Pro

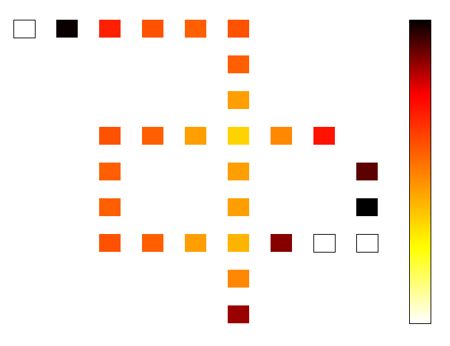


Figure 17: Thermal Energy Disspation Analysis of DLatch uisng QCA Pro

Now, we will discuss some other parameters or factors that will also be considered in QCA, that is area and delay or latency between input and output.

|  |  |  |  |
| --- | --- | --- | --- |
| **Circuit** | **No. of cells** | **Circuit Area(μ)** | **Latency** |
| SR Latch | 72 | 0.1 | 2 clock cycle |
| D Latch | 29 | 0.04 | 1 clock cycle |

Table 8: Comparision Table of Parameters of SR and D Latch

**Conclusion:**

We tried to build circuits such as sequential circuits [SR Latch and D Latch] in QCA. We also configured Thermal Dissipation analysis of SR Latch and D Latch. After seeing the outputs of this latchs we can say that there is a Delay or latency between input and output. That is, SR Latch has latency of 2 clock cycles with occupied area of 0.1μm2 .D latch has latency of 1 clock cycle with occupied area of 0.04 μm2. We also observed that as there is increase in temperature, there is increase in Average Energy Dissipation. Hence, when we compare these parameters with CMOS Technology, they are quite optimized with reduction of area and energy dissipation. Hence this technology will enhance the upcoming world in industrial area. In future there is a scope for this technology to make some efficient models.

1. [↑](#footnote-ref-1)